BACKSIDE OF CHIP IMPLEMENTATION OF REDUNDANCY FUSES AND CONTACT PADS

BACKGROUND OF THE INVENTION

[0001] The present invention is directed to electronic devices and, more particularly, to repairable electronic devices that include redundant regions for replacing defective regions of the device, such as the cells of a semiconductor memory device.

[0002] Semiconductor memory devices, such as dynamic random access memory devices (DRAMs), typically include a semiconductor memory cell array formed of a plurality of memory cells arranged in rows and columns and include a plurality of bit lines as well as a plurality of word lines that intersect the bit lines. Each memory cell of the array is located at the intersection of a respective word line and a respective bit line and includes a capacitor for storing data and a transistor for switching, such as a planar or vertical MOS transistor. The word line is connected to the gate of the switching transistor, and the bit line is connected to the source or drain of the switching transistor. When the transistor of the memory cell is switched on by a signal on the word line, a data signal is transferred from the capacitor of the memory cell to the bit line connected to the memory cell or from the bit line connected to the memory cell to the capacitor of the memory cell.

[0003] As the capacity of semiconductor memory devices increases, the likelihood that a device includes one or more defective memory cells also increases, thereby adversely affecting the yield of the semiconductor memory device manufacturing processes. To address this problem, redundant memory cells are provided which can replace memory cells that are found to be defective during device testing. Typically, one or more spare rows, known as row redundancy, and/or one or more spare columns, known as column redundancy, are included in the memory cell array. The spare rows and/or columns have programmable decoders that can be programmed to respond to the

address of the defective row and/or column, known as the fail address, while at the same time disabling the selection of the defective cell. To program the address of a defective memory cell into the programmable decoder, one or more fuses are programmed to represent the respective bits of the fail address by blowing selected ones of the fuses. One of a 0 or 1 value is defined as a fuse in a blown or open state, and the other of the 0 and 1 values is defined as a fuse in an unblown or shorted state.

[0004] When an address of a defective memory cell is received, the redundant memory cell is selected so that part or all of the word line or bit line that is connected to the redundant memory cell is substituted for the corresponding portion of a word line or bit line of entire word line or bit line that contains the defective memory cell. As a result, the repaired memory device chip cannot be readily distinguished, at least electrically, from a defect-free chip.

[0005] Though semiconductor device elements have become increasingly smaller as the minimum feature size of the device elements has decreased, the total area of the device chip may not significantly decrease because of the presence of other elements on the chip whose size cannot be reduced. As an example, the spacing of the programmable fuse elements described above cannot be reduced below a minimum value, typically 1 μm, because of the laser cutting used to "blow" the fuse elements. A minimum spot size is needed for the incident laser beam to deliver sufficient energy to blow the fuse. Though beams having smaller spot sizes are possible by reducing the wavelength of the beam, the energy of the beam is also reduced and may not be sufficient to ensure cutting of the fuse. Moreover, as the spot size approaches the wavelength of the beam, the beam is prone to diffraction so that the beam cannot be focused on the fuse element.

[0006] Another device element whose size and/or spacing cannot readily be reduced below a minimum size is the bonding pad. When wire bonds are used, the width of the bonding wires

and the size of the solder connections cannot be shrunk without risking breakage of the bonding wires, inadequate solder for the connection or misaligned bonding connections. When the bonding pads directly contact the lead frame, such as for a flip chip device, a minimum spacing between leads is also required.

[0007] It is nevertheless desirable to reduce the total area of the chip despite the limitations of fuse size and spacing and bonding pad size and spacing.

SUMMARY OF THE INVENTION

[0008] The present invention provides a reduction of the total size of the chip by locating the fuses and/or the bonding pads on the backside of the chip and by providing interconnects between circuit elements located on the front side of the chip and the elements located on the backside of the chip.

[0009] In accordance with an aspect of the invention, an electronic device is formed in a substrate. A plurality of circuit elements are formed in a first surface of the substrate. The plurality of circuit elements include at least one active circuit element and at least one redundant circuit element. At least one programmable fuse element is formed in a second surface of the substrate. The programmable fuse element stores, when the active circuit element is defective, an indication thereof. At least one interconnect connects the plurality of circuit elements and the fuse element.

[0010] According to another aspect of the invention, a memory device is formed in a substrate. Circuit elements are formed in a first surface of a substrate and include active memory cells and redundant memory cells. Programmable fuse elements are formed in a second surface of a substrate and store, when at least one of the active memory cells is defective, an address thereof. A plurality of interconnects connects the plurality of circuit elements and the programmable fuse elements.

[0011] According to a further aspect of the invention, an electronic device is formed in a substrate. Circuit elements are formed in a first surface of a substrate. At least one bonding pad is formed in a second surface of a substrate. At least one interconnect connects the plurality of active circuit elements and the bonding pad.

[0012] The foregoing aspects, features and advantages of the present invention will be further appreciated when considered with reference to the following description of the preferred embodiments and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Fig. 1 is a diagram showing a top plan view of a front surface of a known memory circuit chip.

[0014] Fig. 2 is a diagram showing a top plan view of a front surface of a memory circuit chip in accordance with an aspect of the invention.

[0015] Fig. 3 is a schematic diagram showing the interconnection of programmable fuse elements formed on a back surface of the memory chip shown in Fig. 2.

[0016] Fig. 4 is a diagram showing a top plan view of a back surface of a memory circuit chip in accordance with another aspect of the invention.

DETAILED DESCRIPTION

[0017] Fig. 1 shows an example of a known DRAM circuit 110 formed in a top surface of a chip 100 that includes a memory cell array 105. The memory cell array 105 is formed of plural word lines and plural bit lines. Also provided are redundant bit lines or redundant word lines that may be used to replace corresponding portions of defective bit lines or defective word lines.

[0018] The DRAM 110 writes data to or reads data from respective memory cells of the memory cell array 105 as a function of received row and column addresses. Specifically, a control circuit (not shown) receives, via an address bus (not shown), the row and column address of at least one cell of the memory cell array 105 that is to be accessed. The

control circuit then delivers the row address to a row decoder section 102 that drives a selected word line based on a row address signal and delivers the column address to a column decoder section 103 that drives a selected bit line as a function of a column address signal.

[0019] A plurality of fuses 104 is programmed to represent the respective bits of the fail addresses by defining one of a 0 or 1 value as a fuse in a blown or open state, and the other of the 0 and 1 values as a fuse in an unblown or shorted state. When the row decoder section 102 receives a row address or the column decoder section 103 receives a column address that the stored fail address information indicates is defective, the row decoder section 102 or the column decoder section 103 instead activates one or more portions of the redundant bit lines or redundant word lines in place of the defective bit lines or defective word lines.

[0020] The known DRAM chip 100 has the disadvantage that the active elements, such as the memory cell array 105, the row decoder section 102 or the column decoder section 103 may be reduced in size as smaller feature sizes are introduced which each new device generation, but the size of the fuse elements 104 cannot be reduced. Because laser cutting is used to "blow" the fuse elements, a minimum spacing is required between the fuse elements because of the finite spot size of the laser beam. Though the spot size of the beam may be reduced, the energy that is applied to the fuse element is also reduced, thereby increasing the possibility that a fuse element is not blown.

[0021] Additionally, to store all the fail address values, several-thousand fuse elements may be required on each chip and take up a significant portion of the surface area of the chip that therefore cannot be reduced in size.

[0022] The present invention provides a DRAM chip or other device chip in which the fuse elements are provided on the backside of the chip. Fig. 2 illustrates an example of a front surface of a DRAM device 210 formed in a chip 200 in

accordance with an aspect of the invention. The DRAM 210 writes data to or reads data from respective memory cells of a memory cell array 205 using a row decoder section 202 and a column decoder section 203 in the manner described above. However, in place of the fuse elements ordinarily located on the front surface of the chip, the fuse elements are arranged on the back surface of the chip. A plurality of openings allows interconnects to pass from the front surface of the chip to the back surface of the chip, such as openings 220,222,224,226,... through which interconnects pass from the row decoder section 202 on the front surface of the chip to to the fuse elements disposed on the back surface, openings 230,232,234,... through which interconnects pass from the column decoder section 203 on the front surface of the chip to the fuse elements on the back surface, and openings 240,242,244,246,... through which interconnects pass from other circuitry located on the front surface of the chip to the fuse elements on the back surface of the chip.

[0023] The openings through the chip may be generated by any of a number of techniques known in the art, such as chemical etching, laser-assisted etching, electron beam milling or focused ion beam etching. The interconnections through the openings may also be provided using methods known in the art, such as are used for printed circuit boards.

[0024] Fig. 3 schematically illustrates an arrangement of the programmable fuse elements 300 on the back surface of the chip 200. The fuse elements 300 are arranged in a two-dimensional array, and each of the fuse elements 300 provide a unique connection between a respective one of input lines 302 and a respective one of output lines 304 which are also formed on the back surface of the chip. Each of the input lines 302 is connected via a respective one of the openings 240,242,244,246,... to control circuitry (not shown) located on the front side of the chip. Each of the output lines 304 is connected via a respective one of the openings 220,222,224,226,... to the row decoder section 202 or via a

respective one of the openings 230,232,234,... to the column decoder section 203. The programmable fuse elements, the input lines and the output lines may be formed on the back surface of the chip using known processing methods.

[0025] The information stored in the fuse elements 300 is read by sequentially activating each of the input lines 302 and then reading the output generated at one of the output lines 304. As an example, to read the values stored in the uppermost row of fuses 300, an input line connected to the front surface of the chip through the opening 240 is activated, then an input line connected to the opening 242 is activated, an input line connected to the opening 244 is next activated, and thereafter an input line connected to the opening 246 is activated. As each of the input lines 302 is activated, an output is read at the line connected to opening 222. Similarly, the values stored in the second row of fuses are read from the outputs of the line connected to the opening 224, the values stored in the third row of fuses are read from the line connected to the opening 226, the values stored in the fourth row of fuses are read using the line connected to the opening 228, etc. Various circuitry known in the art may be incorporated on the front surface of the chip and connected to these openings to control the reading operation.

[0026] Fig. 4 illustrates an alternative embodiment of the invention in which bonding pads 420 of a DRAM circuit chip or other circuit chip are disposed on the back surface of a chip 400. A plurality of openings 410 that extend from the front surface of a chip to the back surface of a chip permit interconnection 430 to pass from the circuitry on the front surface of a chip to the bonding pads 420 on the back surface of the chip. Fig. 4 illustrates only one of many possible arrangements of the bonding pads on the back surface of a chip.

[0027] Advantageously, the invention allows for reductions in chip size without reducing the size or spacing of the fuse elements or the size or spacing of the bonding pads. As a

result, a greater number of chips may be formed on a single wafer without sacrificing processing reproducibility or device reliability.

[0028] Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as defined by the appended claims.